CLAIMS

1-17. (canceled)

18. (new) A phase-locked loop (PLL) circuit comprising:

(a) a frequency synthesis section comprising:

(1) a voltage-controlled oscillator (VCO) adapted to generate a PLL output signal for the PLL circuit based on a control voltage signal applied at an input of the VCO;

(2) a loop filter connected to the VCO input;

(3) a phase frequency detector (PFD) adapted to compare a feedback signal derived from the PLL output signal to a reference signal;

(4) a charge pump adapted to generate charge based on output signals from the PFD; and

(5) a first switch adapted to selectively connect the charge pump to the loop filter;

(b) a direct frequency control section comprising:

(1) a look-up table (LUT) adapted to store digital data values representing a plurality of tuning voltages corresponding to different frequencies for the PLL output signal;

(2) a first tuning section adapted to convert a digital data value received from the LUT into a corresponding tuning voltage for the VCO;

(3) a second switch adapted to selectively connect the first tuning section to the VCO input to selectively apply the corresponding tuning voltage from the first tuning section as the control voltage signal for the VCO;

(4) a second tuning section adapted to generate a digital data value for the LUT corresponding to the control voltage signal applied to the VCO input; and

(5) a third switch adapted to selectively connect the VCO input to the second tuning section to selectively enable the second tuning section to update the LUT based on the generated digital data value; and

(c) a controller adapted to control the first, second, and third switches.

19. (new) The invention of claim 18, wherein the first tuning section comprises:

a digital-to-analog converter (DAC) adapted to convert the digital data value received from the LUT into an analog signal; and

a first operational amplifier (op-amp) adapted to generate the corresponding tuning voltage from the analog signal; and

20. (new) The invention of claim 19, wherein the second tuning section comprises:

a second op-amp adapted to sense the control voltage signal applied to the VCO input;

an analog-to-digital converter (ADC) adapted to convert the sensed control voltage signal from the second op-amp into the corresponding digital data value for the LUT.

21. (new) The invention of claim 18, wherein the second tuning section comprises:

a second op-amp adapted to sense the control voltage signal applied to the VCO input;

an ADC adapted to convert the sensed control voltage signal from the second op-amp into the corresponding digital data value for the LUT.

22. (new) The invention of claim 18, wherein the controller is adapted to control operations of the PLL in first, second, and third modes such that:

in the first mode, the first switch is closed and the second and third switches are open, such that the frequency synthesis section generates the control voltage signal for the VCO;

in the second mode, the second switch is closed and the first and third switches are open, such that the direct frequency control section generates the control voltage signal for the VCO; and

in the third mode, the first and third switches are closed and the second switch is open, such that the frequency synthesis section generates the control voltage signal for the VCO, while the direct frequency control section updates the LUT.

23. (new) The invention of claim 22, wherein the controller is adapted to:

transition from the first mode to the second mode when the frequency of the PLL output signal is to be changed from a current frequency to a different, desired frequency; and

transition from the second mode back to the first mode after the controller determines that the PLL output signal has sufficiently achieved the desired frequency.

24. (new) The invention of claim 22, wherein, when the PLL is in the third mode, the controller is adapted to sequentially select a plurality of different frequencies for the PLL output signal to generate a plurality of different digital data values for the LUT.

25. (new) The invention of claim 22, wherein the controller is further adapted to control operations of the PLL in a fourth mode, wherein the first and second switches are closed and the third switch is open, such that the frequency synthesis generates a first portion of the control voltage signal for the VCO, while the direct frequency control section generates a second portion of the control voltage signal for the VCO.

26. (new) The invention of claim 25, wherein:

the first tuning section comprises:

(i) a digital-to-analog converter (DAC) adapted to convert the digital data value received from the LUT into an analog signal; and

(ii) a first operational amplifier (op-amp) adapted to generate the corresponding tuning voltage from the analog signal; and

the second tuning section comprises:

(i) a second op-amp adapted to sense the control voltage signal applied to the VCO input;

(ii) an analog-to-digital converter (ADC) adapted to convert the sensed control voltage signal from the second op-amp into the corresponding digital data value for the LUT;

the controller is adapted to:

(i) transition from the first mode to the second mode when the frequency of the PLL output signal is to be changed from a current frequency to a different, desired frequency; and

(ii) transition from the second mode back to the first mode after the controller determines that the PLL output signal has sufficiently achieved the desired frequency; and

when the PLL is in the third mode, the controller is adapted to sequentially select a plurality of different frequencies for the PLL output signal to generate a plurality of different digital data values for the LUT.